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| Image result for adamas university logo | **ADAMAS UNIVERSITY**  **END SEMESTER EXAMINATION**  (Academic Session: 2020 – 21) | | |
| **Name of the Program:** | BSC | **Semester:** | I |
| **Paper Title:** | Computer Organization | **Paper Code:** | ECS31193 |
| **Maximum Marks:** | 50 | **Time Duration:** | 3 Hrs |
| **Total No. of Questions:** | **17** | **Total No of Pages:** | 3 |
| *(Any other information for the student may be mentioned here)* | 1. At top sheet, clearly mention Name, Univ. Roll No., Enrolment No., Paper Name & Code, Date of Exam. 2. All parts of a Question should be answered consecutively. Each Answer should start from a fresh page. 3. Assumptions made if any, should be stated clearly at the beginning of your answer. | | |

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| **Group A**  **Answer All the Questions (5 x 1 = 5)** | | | |
| 1 | A source program is usually in \_\_\_\_\_\_\_ a) Assembly language b) Machine level language c) High-level language d) Natural language | **R** | **CO1** |
| 2 | Which memory device is generally made of semiconductors? a) RAM b) Hard-disk c) Floppy disk d) Cd disk | **R** | **CO2** |
| 3 | The small extremely fast, RAM’s are called as \_\_\_\_\_\_\_ | **R** | **CO3** |
| 4 | The ALU makes use of \_\_\_\_\_\_\_ to store the intermediate results. a) Accumulators b) Registers c) Heap d) Stack | **R** | **CO4** |
| 5 | The control unit controls other units by generating \_\_\_\_ a) Control signals b) Timing signals c) Transfer signals d) Command Signals | **R** | **CO5** |
| **Group B**  **Answer Allthe Questions (5 x 2 = 10)** | | | |
| 6 a) | Let us assume that a complete execution of a program requires the execution of 100 machine language instruction. Some instructions may be executed more than once when they are inside loop, So we can assume that the average no of basic steps needed to execute one basic instruction is 7, such that each and every basic step completes in 1 clock cycle. If a 10 Hz – processor is used then calculate time required by the processor to execute the program. | **AP** | **CO1** |
| **(OR)** | | | |
| 6 b) | What is Processor clock. | **R** | **CO1** |
| 7 a) | Explain the role of each and every stage of a four stage general pipeline. | **U** | **CO2** |
| **(OR)** | | | |
| 7 b) | What are the different types of hazards that can occur in a pipeline? | **R** | **CO2** |
| 8 a) | What do you understand by byte addressability. | **R** | **CO3** |
| **(OR)** | | | |
| 8 b) | Discuss the basic functional units of a computer. | **U** | **CO3** |
| 9 a) | Write the instruction sequences for push mechanism in Stack. |  | **CO4** |
| **(OR)** | | | |
| 9 b) | Write the instruction sequences for pop mechanism in Stack. | **R** | **CO4** |
| 10 a) | Explain different formats of instructions with example. | **U** | **CO5** |
| **(OR)** | | | |
| 10 b) | What do you understand by effective address of an operand and explain how it is calculated. | **R** | **CO5** |
| **Group C**  **Answer All the Questions (7 x 5 = 35)** | | | |
| 11 a) | Design an algorithm for division along with the flowchart. | **An** | **CO1** |
| **(OR)** | | | |
| 11 b) | Represent each and every step for dividing 4 by 2 using division algorithm. | **An** | **CO1** |
| 12 a) | Generate the3-Address and 1-Address Instruction sequence for the following expression | **Ap** | **CO2** |
| **(OR)** | | | |
| 12 b) | Generate the 2-Address and Zero address Instruction sequence for the following expression | **AP** | **CO2** |
| 13 a) | Explain the working principle of a synchronous bus for input operation with timing diagram. | **U** | **CO3** |
| **(OR)** | | | |
| 13 b) | What is an interupt and how it is processed | **R** | **CO3** |
| 14 a) | Discuss with with diagram the working principle of a peripheral device | **U** | **CO4** |
| **(OR)** | | | |
| 14 b) | Discuss the process by which input is taken from a keyboard. | **U** | **CO4** |
| 15 a) | What is Instruction Pipeline. What are the reasons for data hazard? Give a solution for data hazard.  A Pipelined processor has 4 stages, Fetch, Decode, Execute, Write Back. Fetch, Decode and Write Back stage takes 1 clock cycle for each and every instructions and for Execution stage it depends on the Instruction. Addition and Subtraction instruction takes 1 clock cycle and Multiplication Instruction takes 3 clock cycles. The Instructions are    I2 : MUL R4 R3 R2  I3 : SUB R5 R4 R2  Calculate the total number of clock cycles required to complete the execution of above Instruction sequence in- *Case1:* Without data forwarding and *Case2:* With data forwarding. | **E** | **CO4** |
| **(OR)** | | | |
| 15 b) | A 4-Stage asynchronous pipelined processor with Fetch, Decode, Execute & Write Back Stages with an instruction sequence with respective clock cycles for every stages is displayed below:   |  |  |  |  |  | | --- | --- | --- | --- | --- | |  | **IF** | **ID** | **EX** | **WB** | | **I1** | 2 | 1 | 1 | 1 | | **I2** | 1 | 3 | 2 | 2 | | **I3** | 1 | 1 | 1 | 3 | | **I4** | 1 | 2 | 2 | 2 |   Calculate the number of clock cycles needed to execute the loop [ **for(i=0;i<=2;i++){I1;I2;I3;I4;}** ]. State briefly the mechanism of processing Instructions in every stages. | **E** | **CO4** |
| 16 a) | Discuss the Internal Organization of the bit cells in a memory chip with diagram. | **An** | **CO5** |
| **(OR)** | | | |
| 16 b) | State the working principle of a CMOS Static RAM cell | **C** | **CO5** |
| 17 a) | The size of the physical address space of a processor is 2P bytes. The word length is 2W bytes. The capacity of cache memory is 2N bytes. The size of each cache block is 2M words. For a K-way set-associative cache memory, what will be the length (in number of bits) of the tag field. | **E** | **CO5** |
| **(OR)** | | | |
| 17 b) | A computer has a 256 KB, 4-way set associative, write back data cache with block size of 32 bytes. The processor sends 32 bit addresses to the cache controller. Each cache tag directory entry contains in addition to address tag, 2 valid bits, 1 modified bit and 1 replacement bit. What do you mean by 4-way set associative cache(with diagram)? Calculate the number of bits in every required field in an address to access the cache memory and the size of the cache tag directory. | **E** | **CO5** |